

FIG. 1

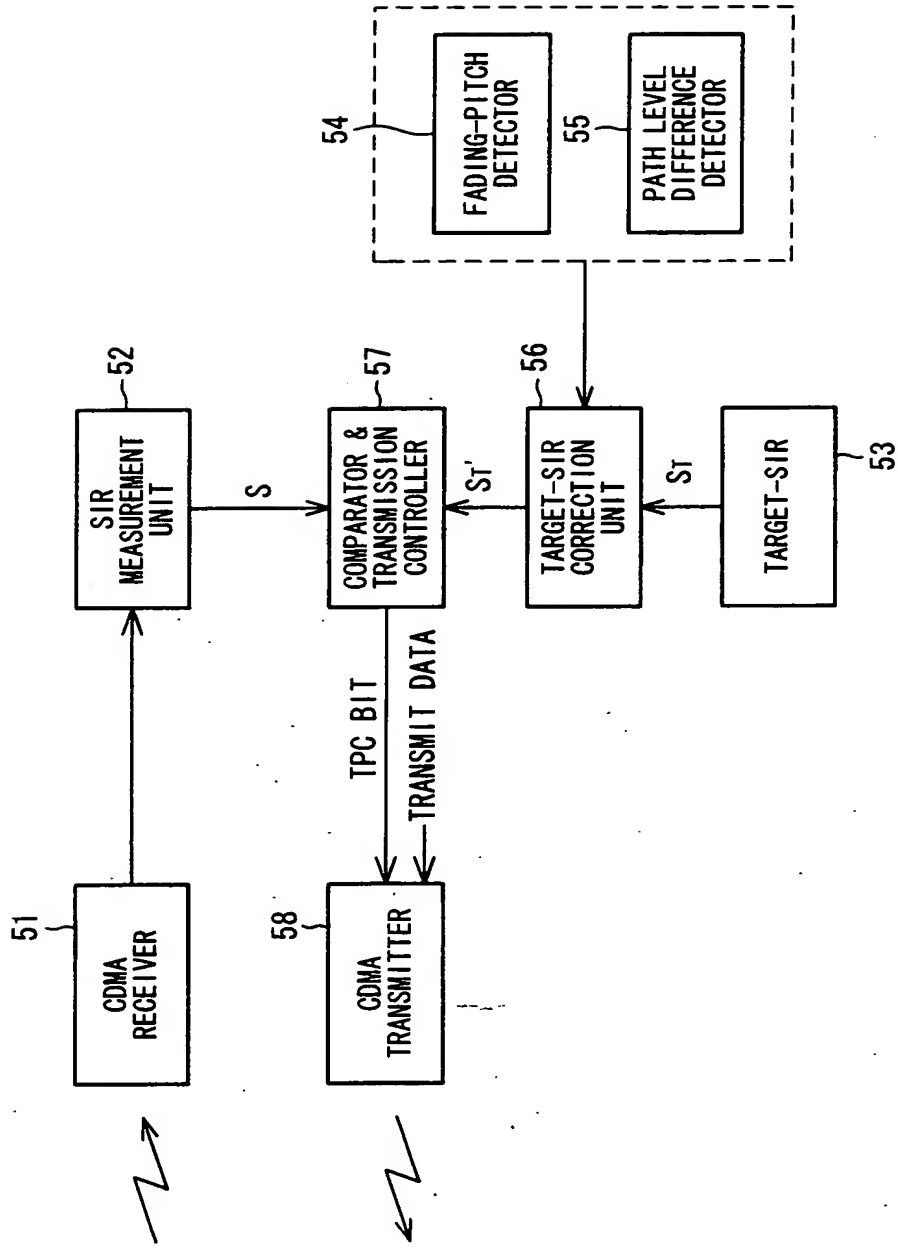
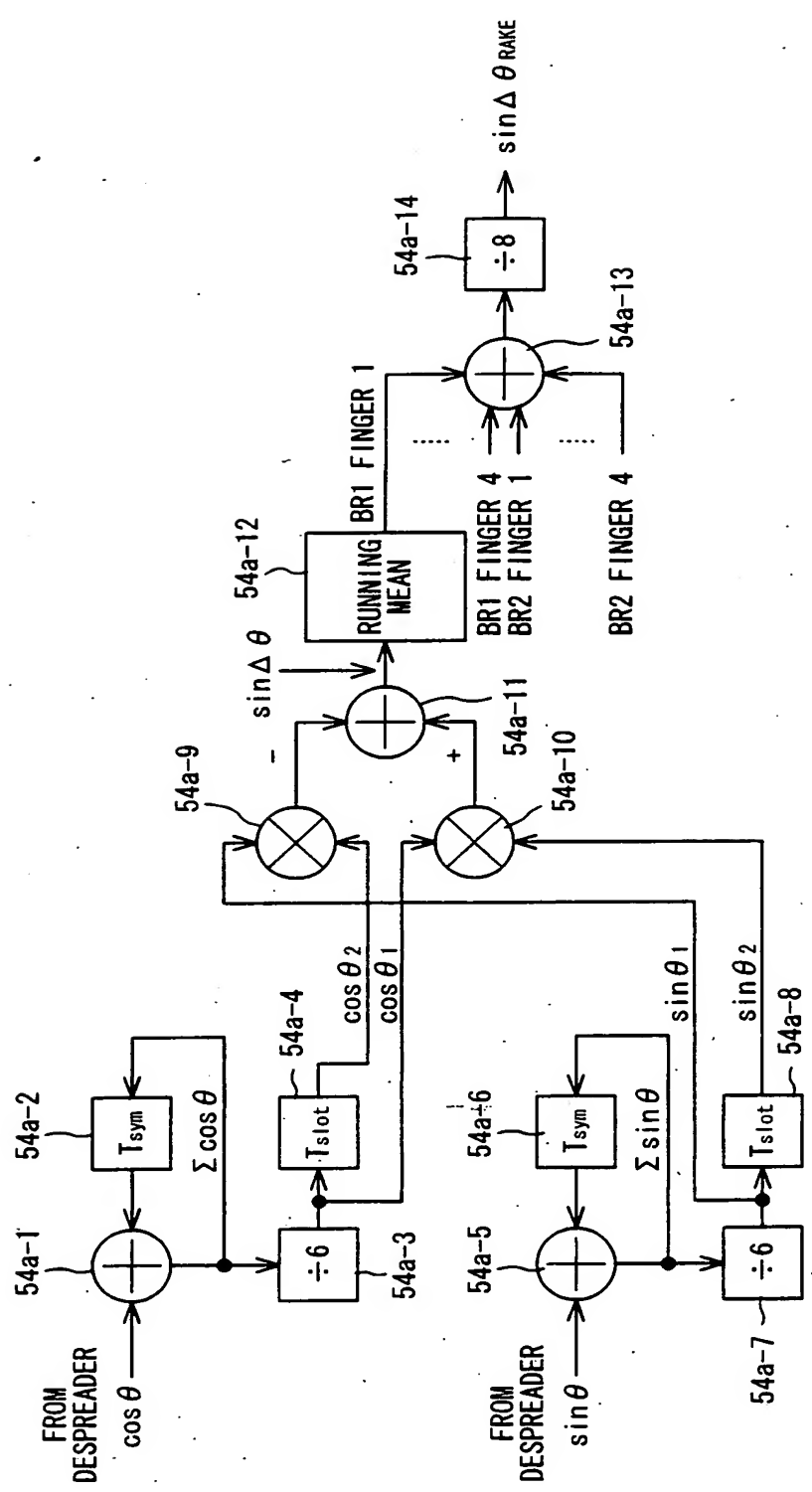


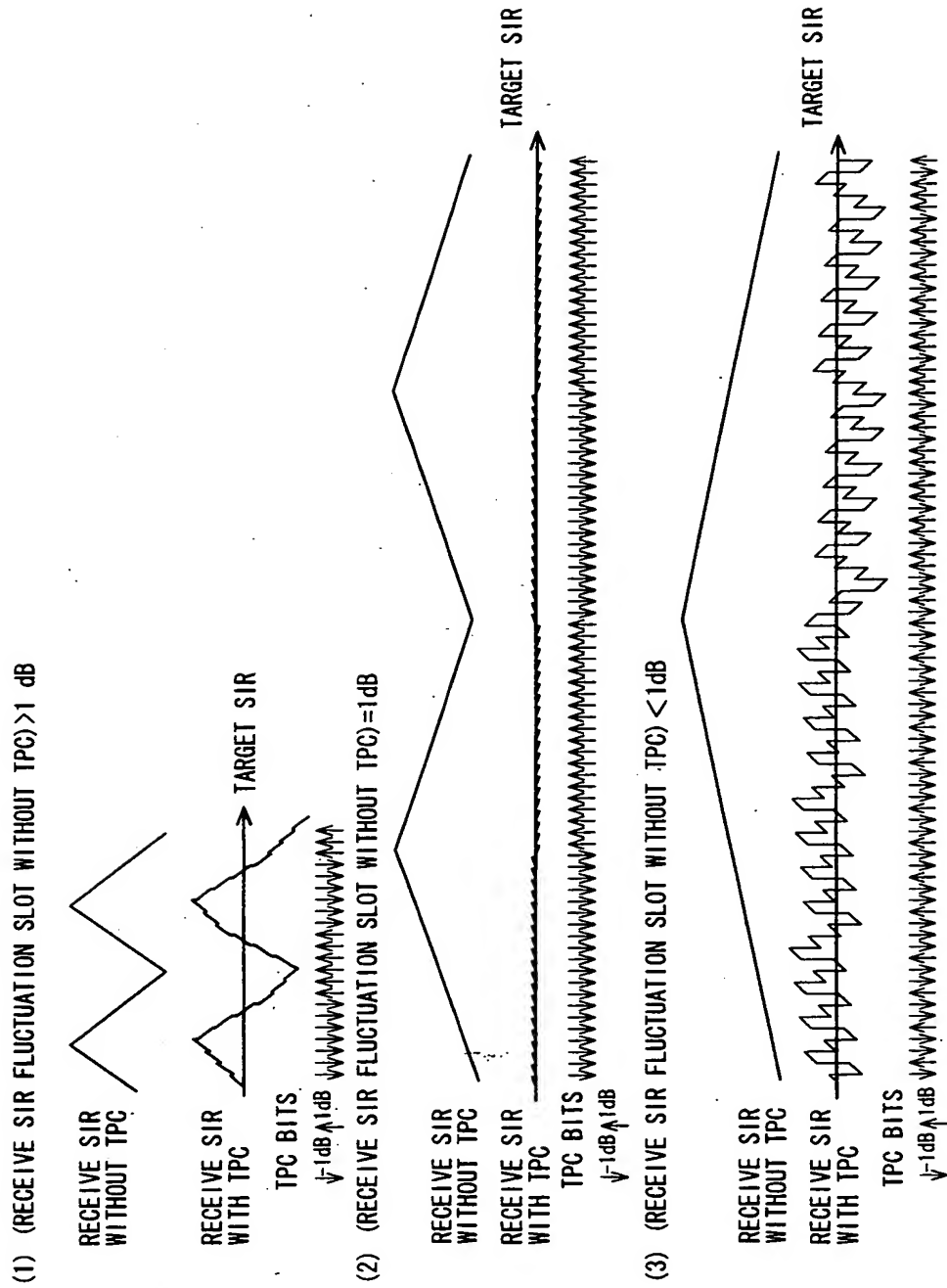
FIG. 2



T_{sym} : ONE SYMBOL DELAY T_{slot} : ONE SLOT DELAY

FIG. 3

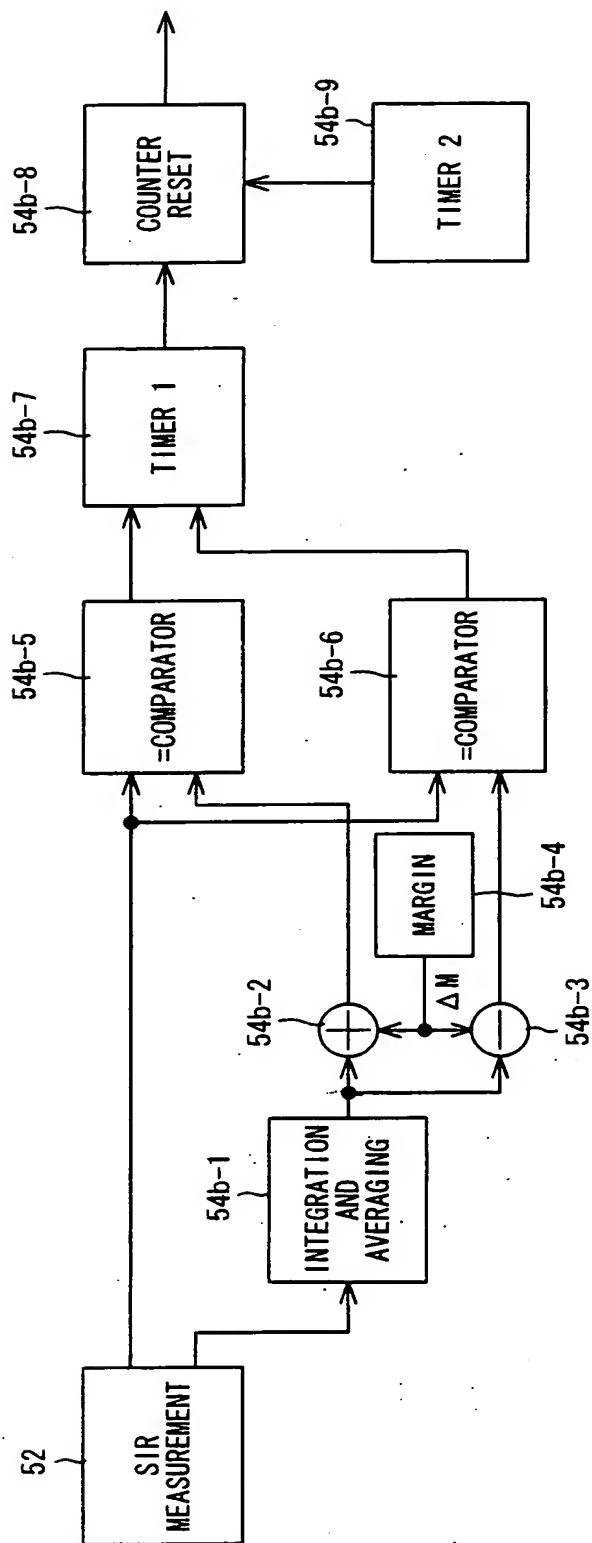
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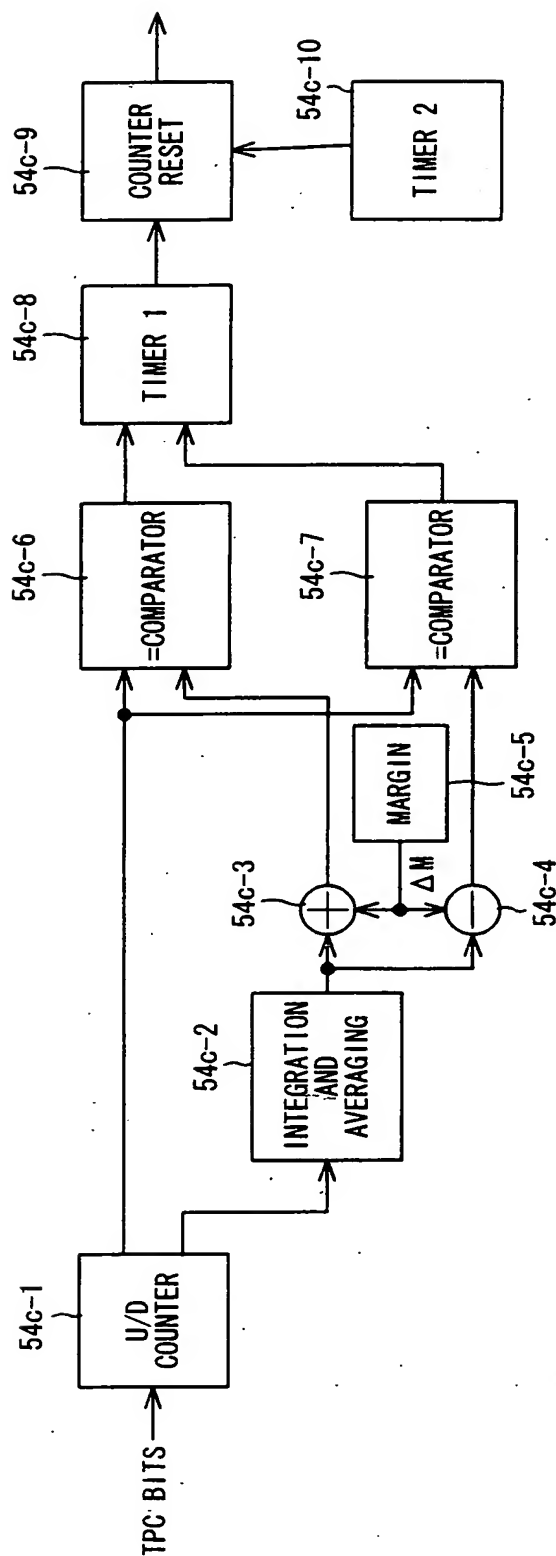
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FIG. 4



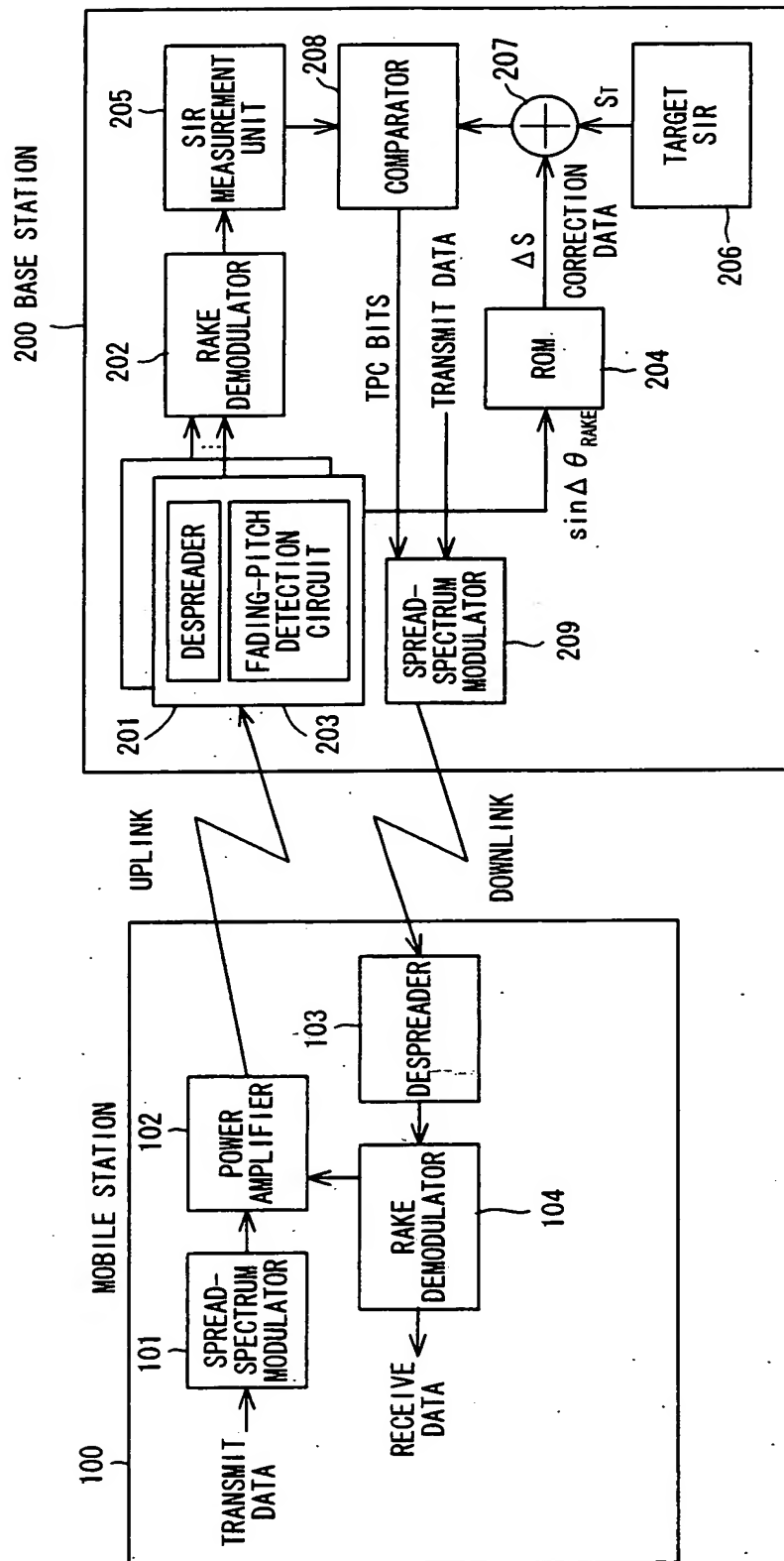
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FIG. 5



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FIG. 6

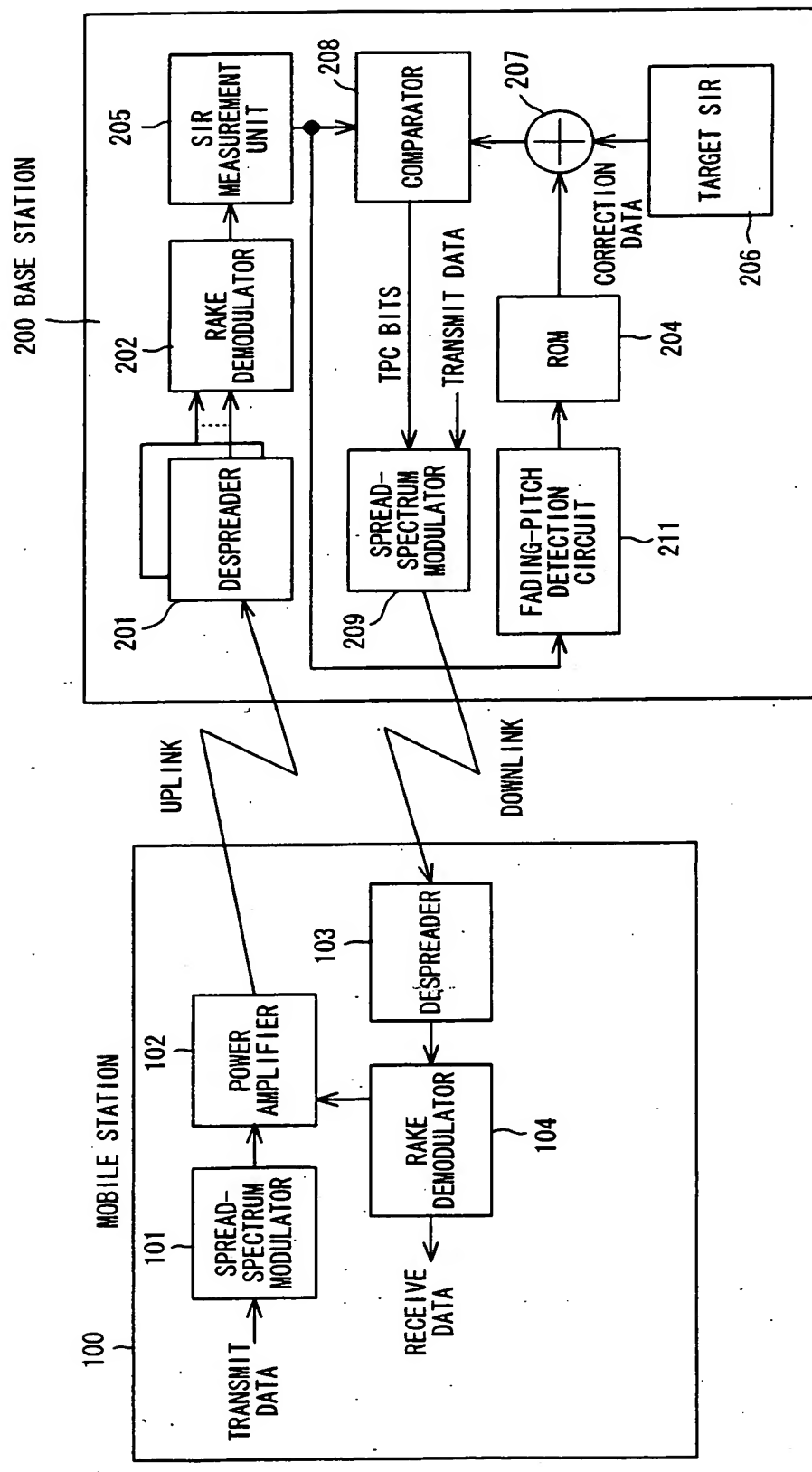


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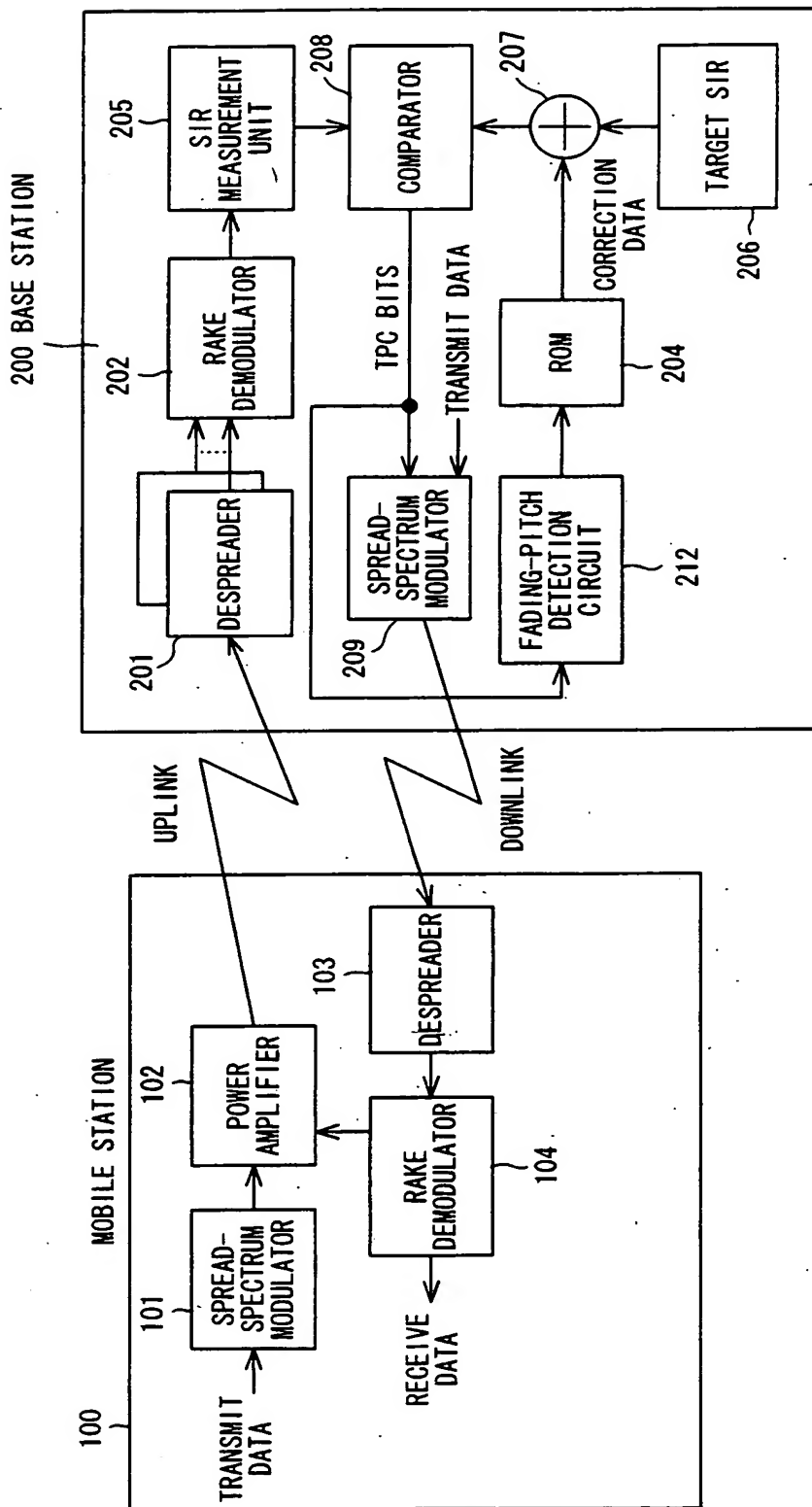
FIG. 7



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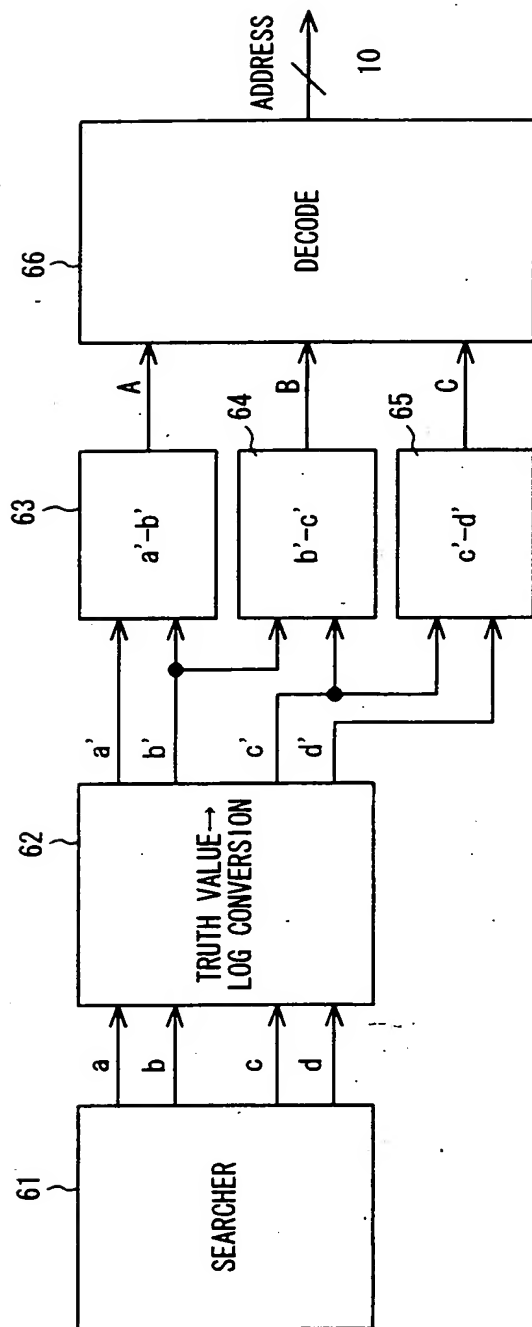
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FIG. 8



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FIG. 9



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FIG. 10

ADDRESS	LEVEL DIFFERENCE (dB) A BETWEEN PATHS 1 AND 2	LEVEL DIFFERENCE (dB) B BETWEEN PATHS 2 AND 3	LEVEL DIFFERENCE (dB) C BETWEEN PATHS 3 AND 4
0	15	0	0
1	14	0	1
2	14	1	0
3	13	0	0
4	13	0	1
5	13	0	2
6	13	1	0
7	13	1	1
8	13	2	0
9	12	0	0
10	12	0	1
11	12	0	2
12	12	0	3
13	12	1	0
14	12	1	1
15	12	1	2
16	12	2	0
17	12	2	1
18	12	3	0
19	11	0	0
20	11	0	1
21	11	0	2
22	11	0	3
23	11	0	4
24	11	1	0
25	11	1	1
26	11	1	2
27	11	1	3
28	11	-2	0
29	11	2	1
30	11	2	2
31	11	3	0
32	11	3	1
33	11	4	0
34	10	0	0
35	10	0	1
36	10	0	2
37	10	0	3
38	10	0	4
39	10	0	5
40	10	1	0
41	10	1	1
42	10	1	2

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FIG. 11

	A	B	C
770	0	7	0
771	0	7	1
772	0	7	2
773	0	7	3
774	0	7	4
775	0	7	5
776	0	7	6
777	0	7	7
778	0	7	8
779	0	8	0
780	0	8	1
781	0	8	2
782	0	8	3
783	0	8	4
784	0	8	5
785	0	8	6
786	0	8	7
787	0	9	0
788	0	9	1
789	0	9	2
790	0	9	3
791	0	9	4
792	0	9	5
793	0	9	6
794	0	10	0
795	0	10	1
796	0	10	2
797	0	10	3
798	0	10	4
799	0	10	5
800	0	11	0
801	0	11	1
802	0	11	2
803	0	11	3
804	0	11	4
805	0	12	0
806	0	12	1
807	0	12	2
808	0	12	3
809	0	13	0
810	0	13	1
811	0	13	2
812	0	14	0
813	0	14	1
814	0	15	0

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FIG. 12

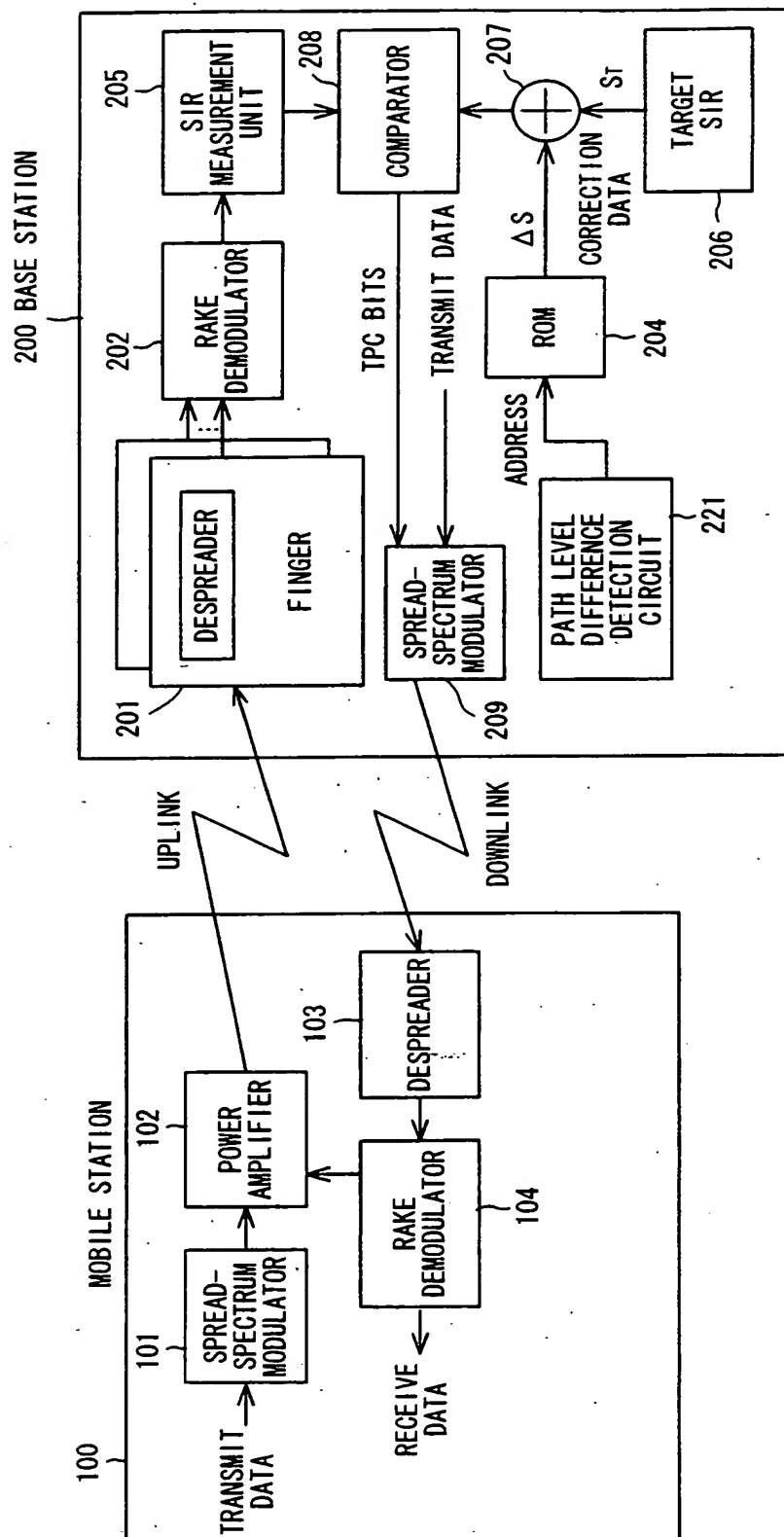


FIG. 13

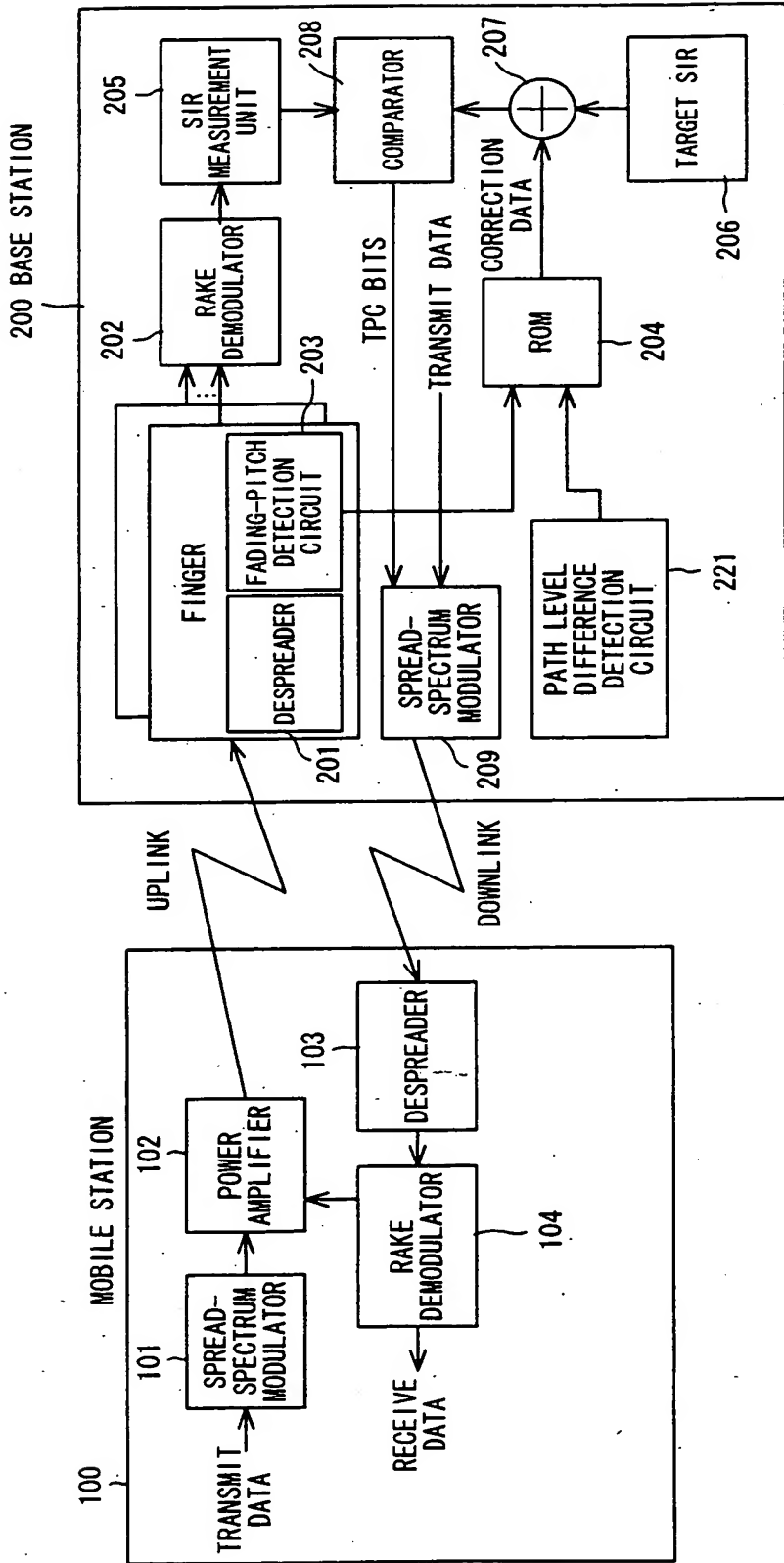


FIG. 14

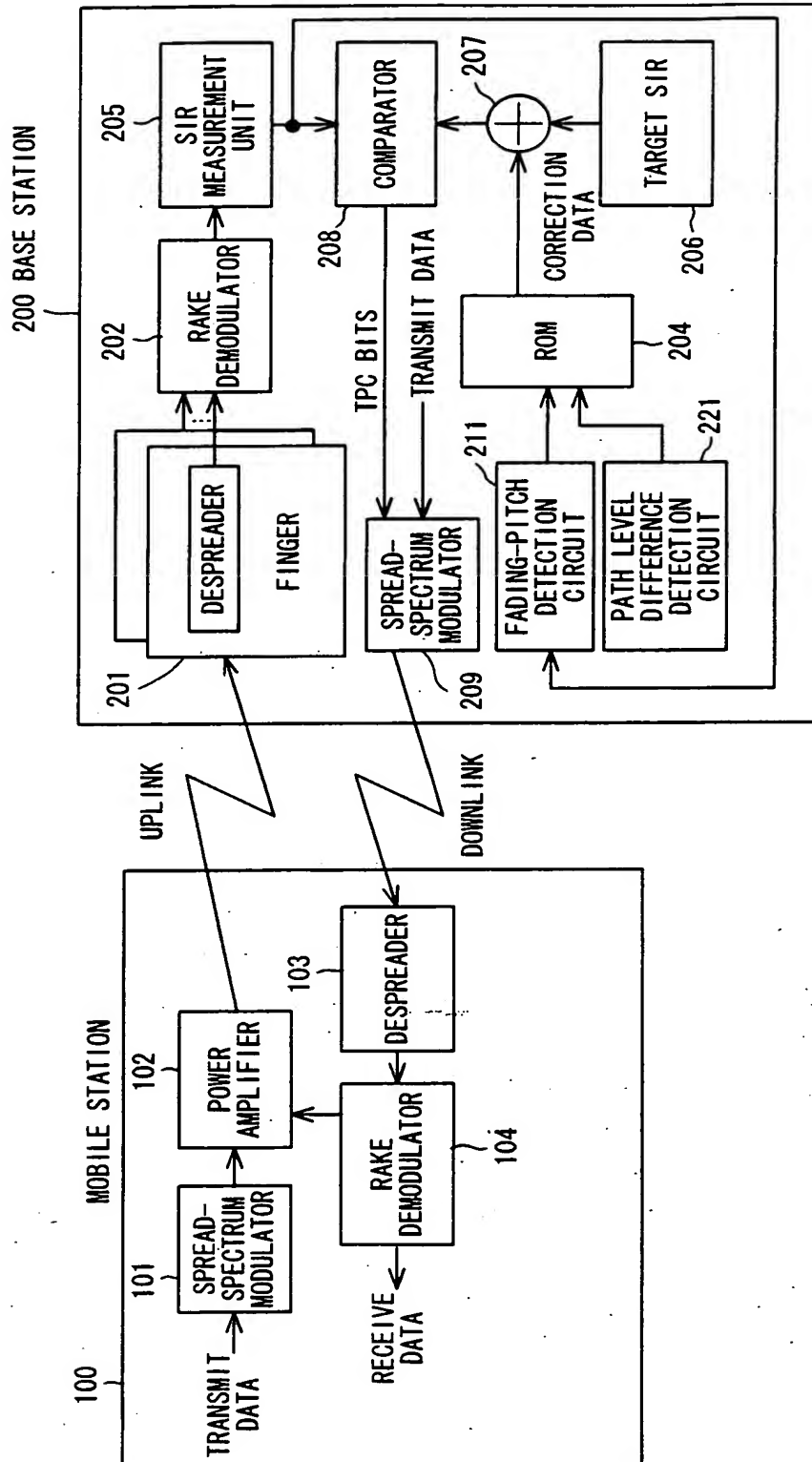


FIG. 15

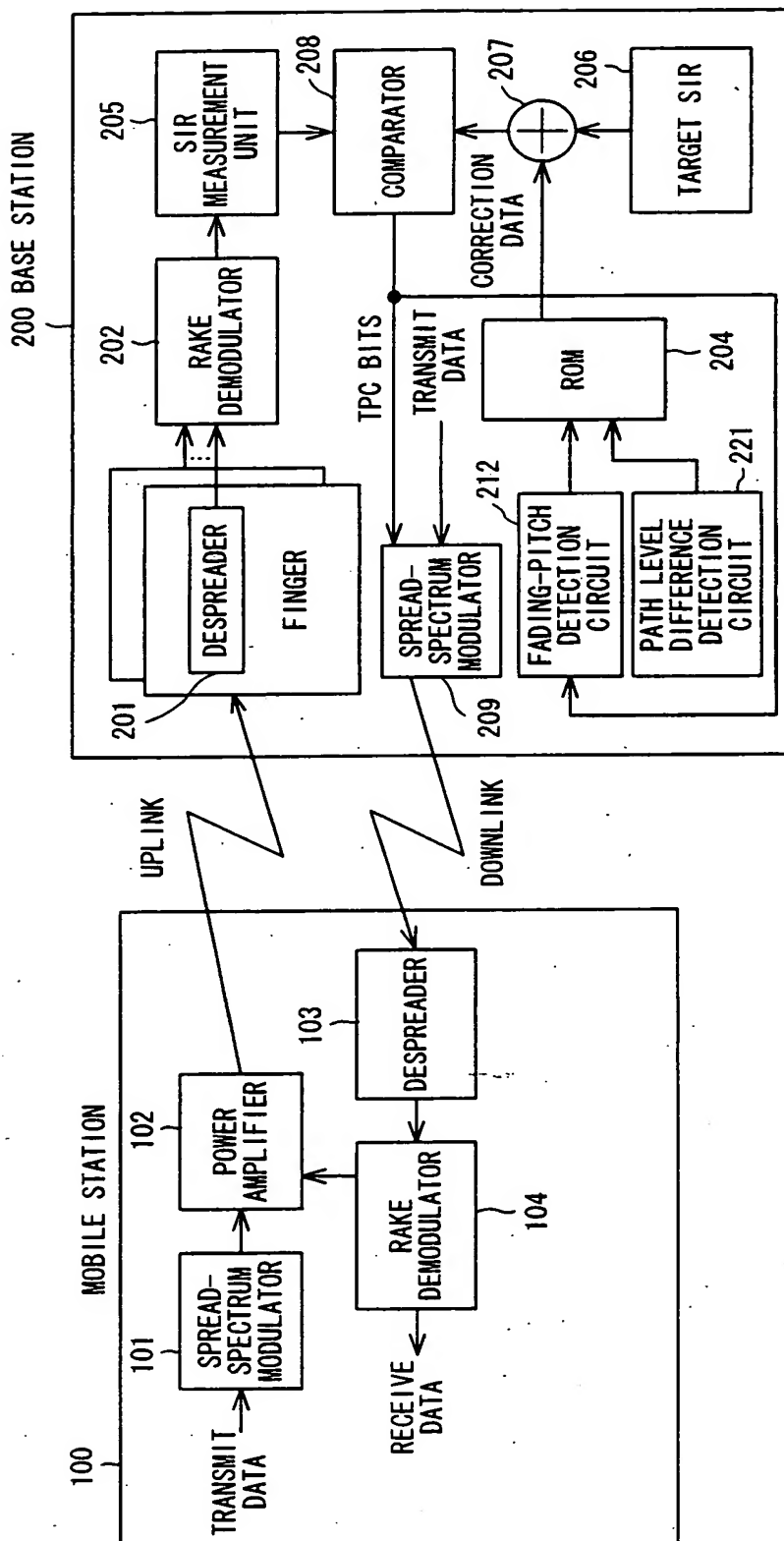


FIG. 16

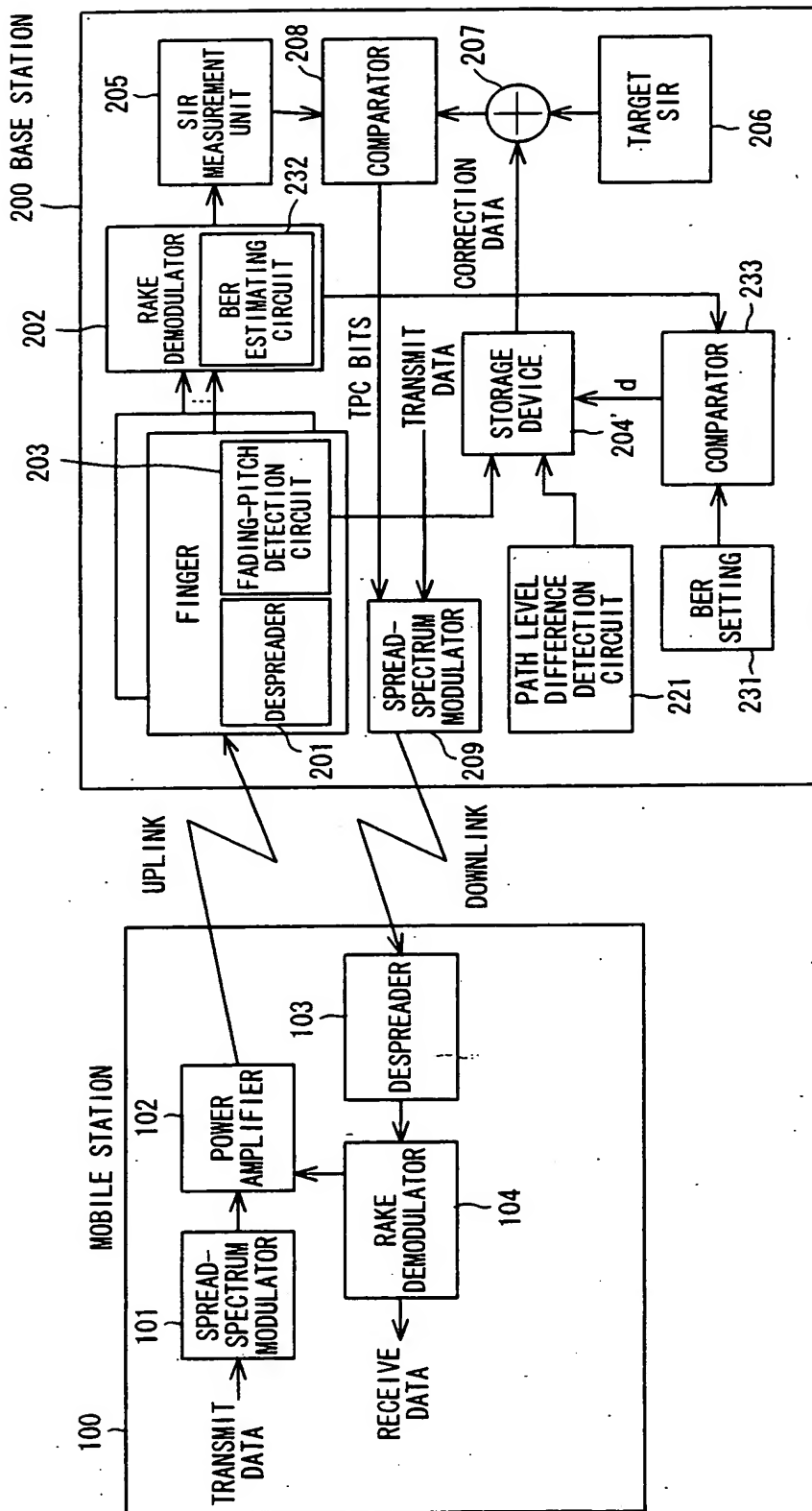


FIG. 17

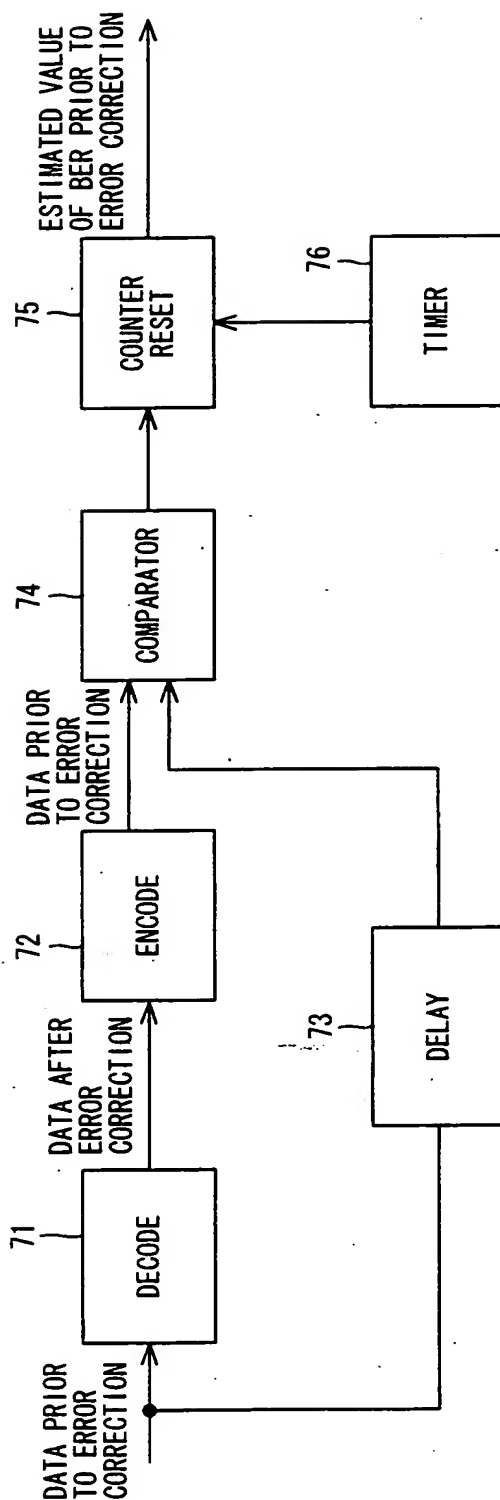


FIG. 18

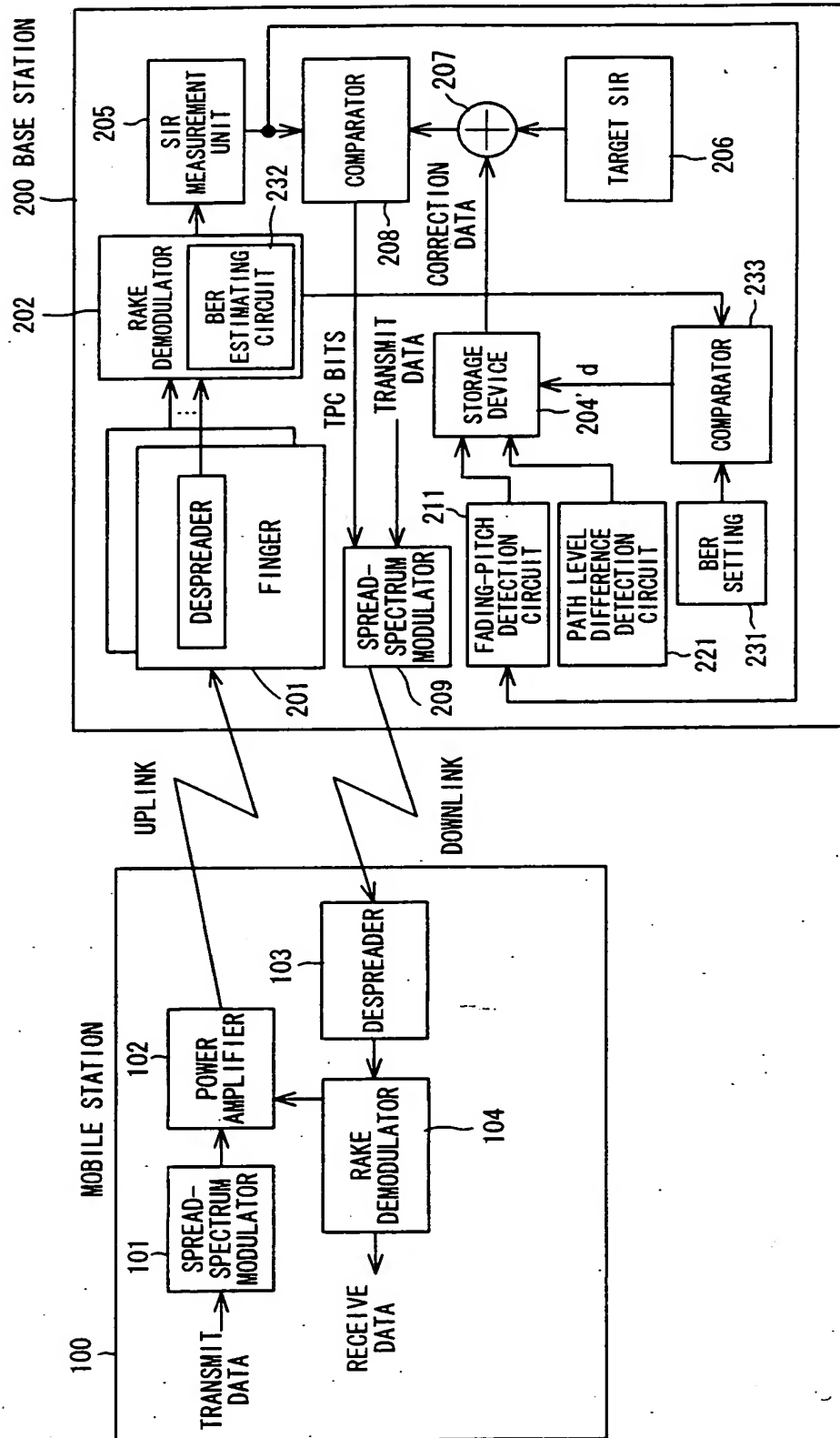


FIG. 19

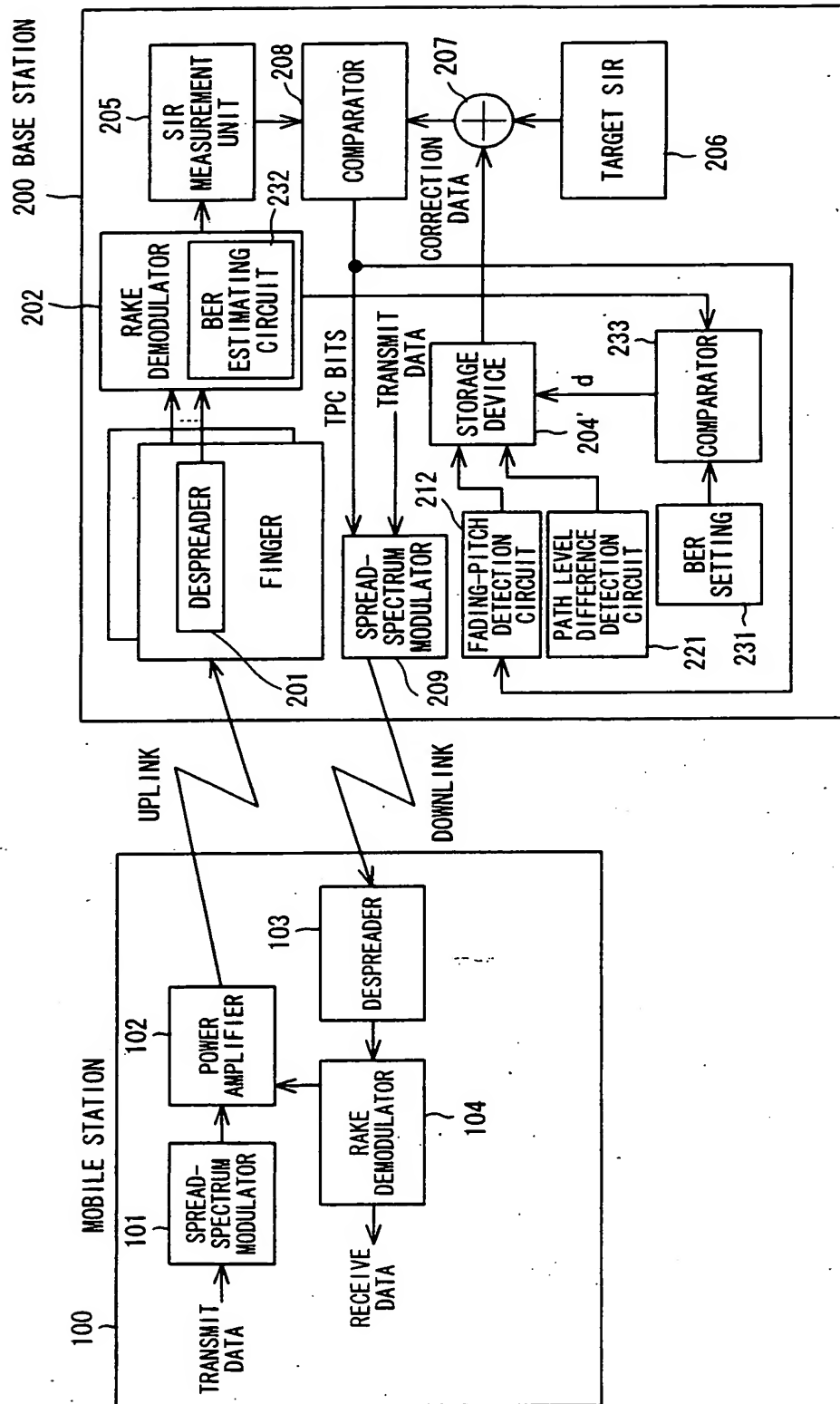


FIG. 20

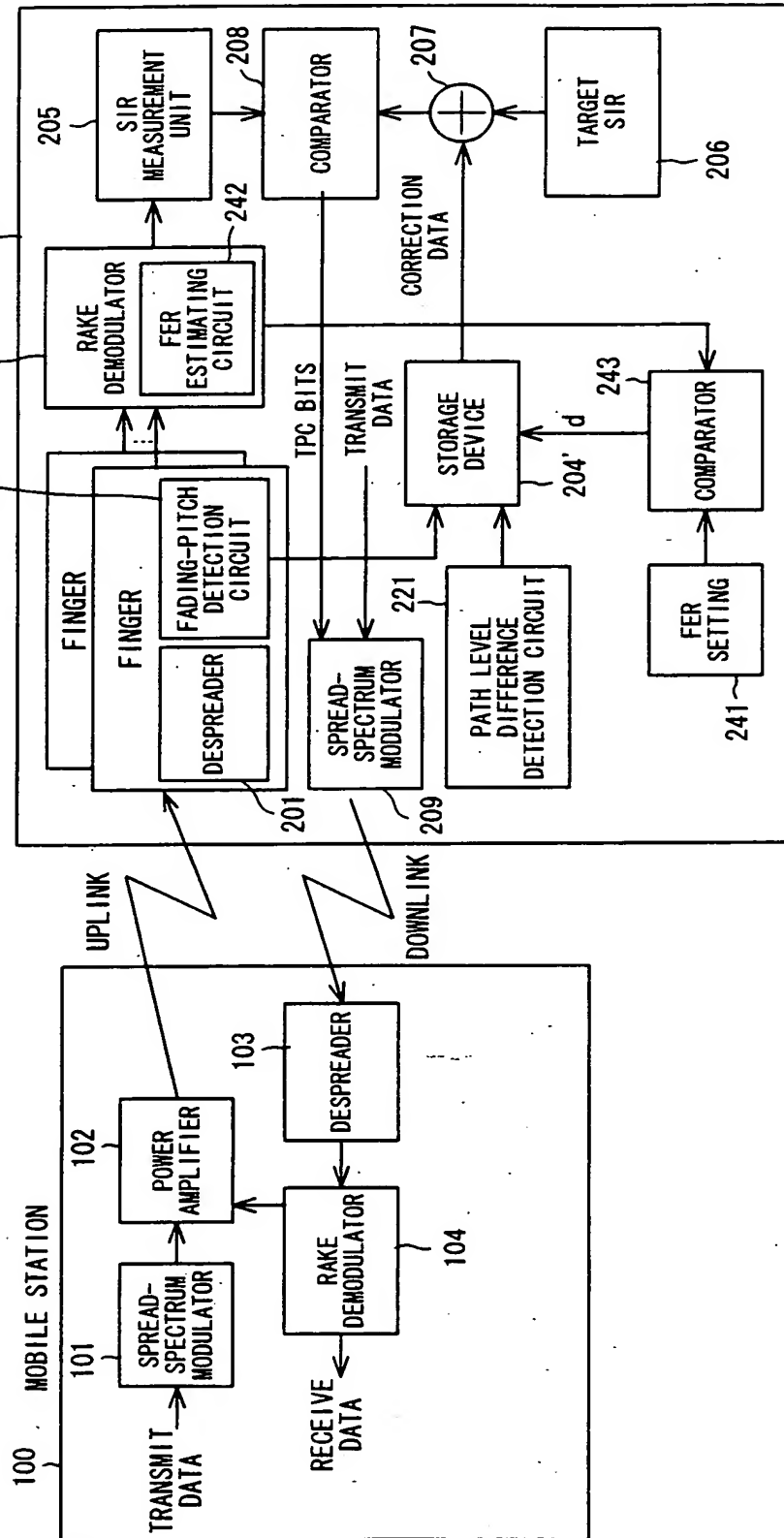


FIG. 21

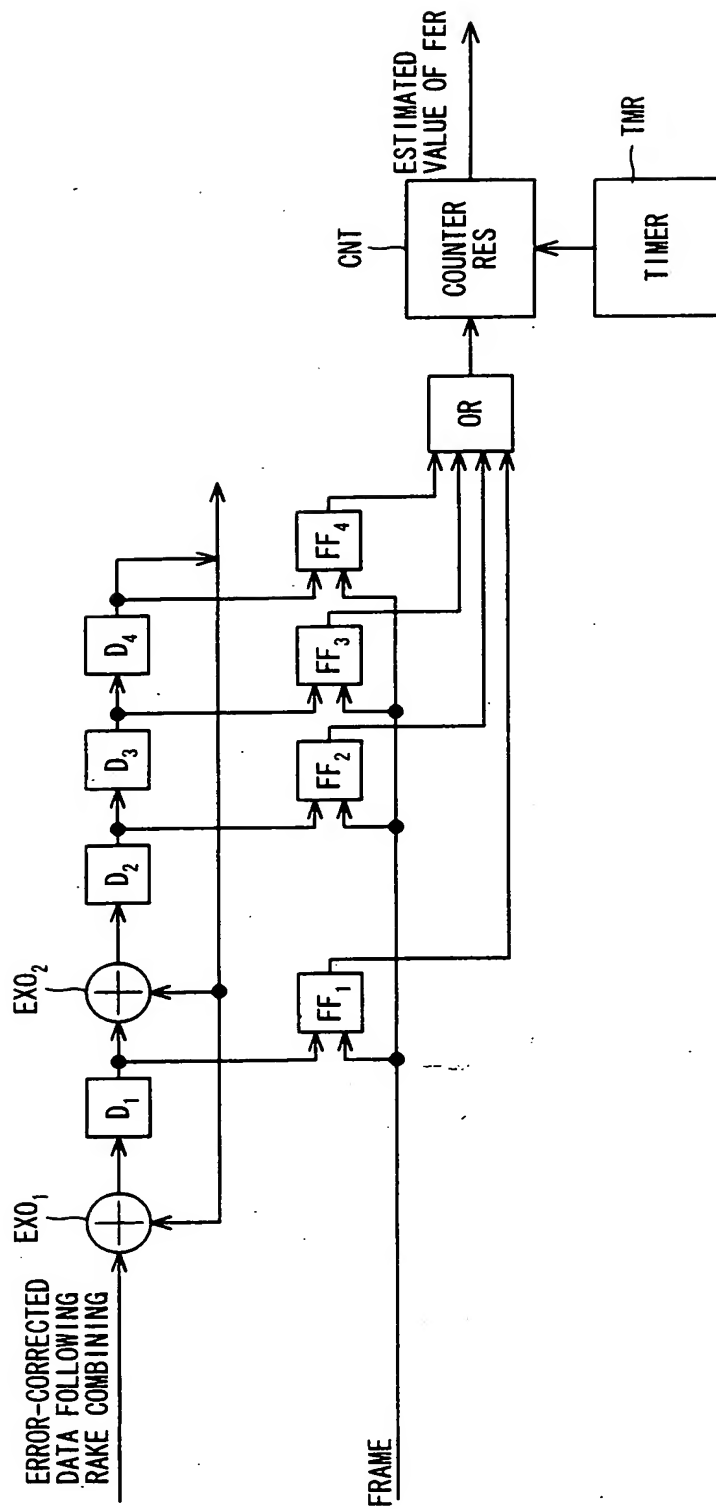


FIG. 22

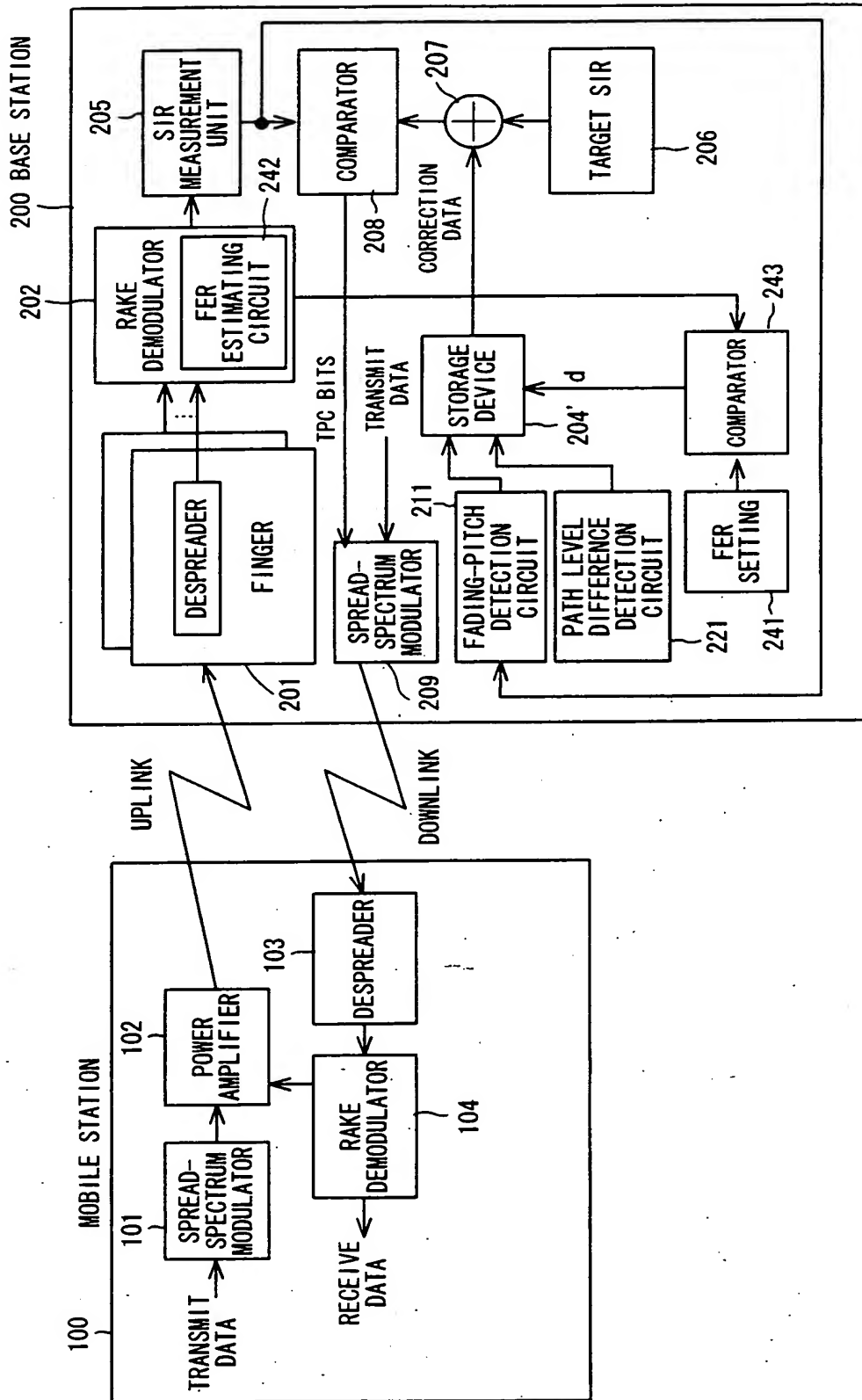


FIG. 23

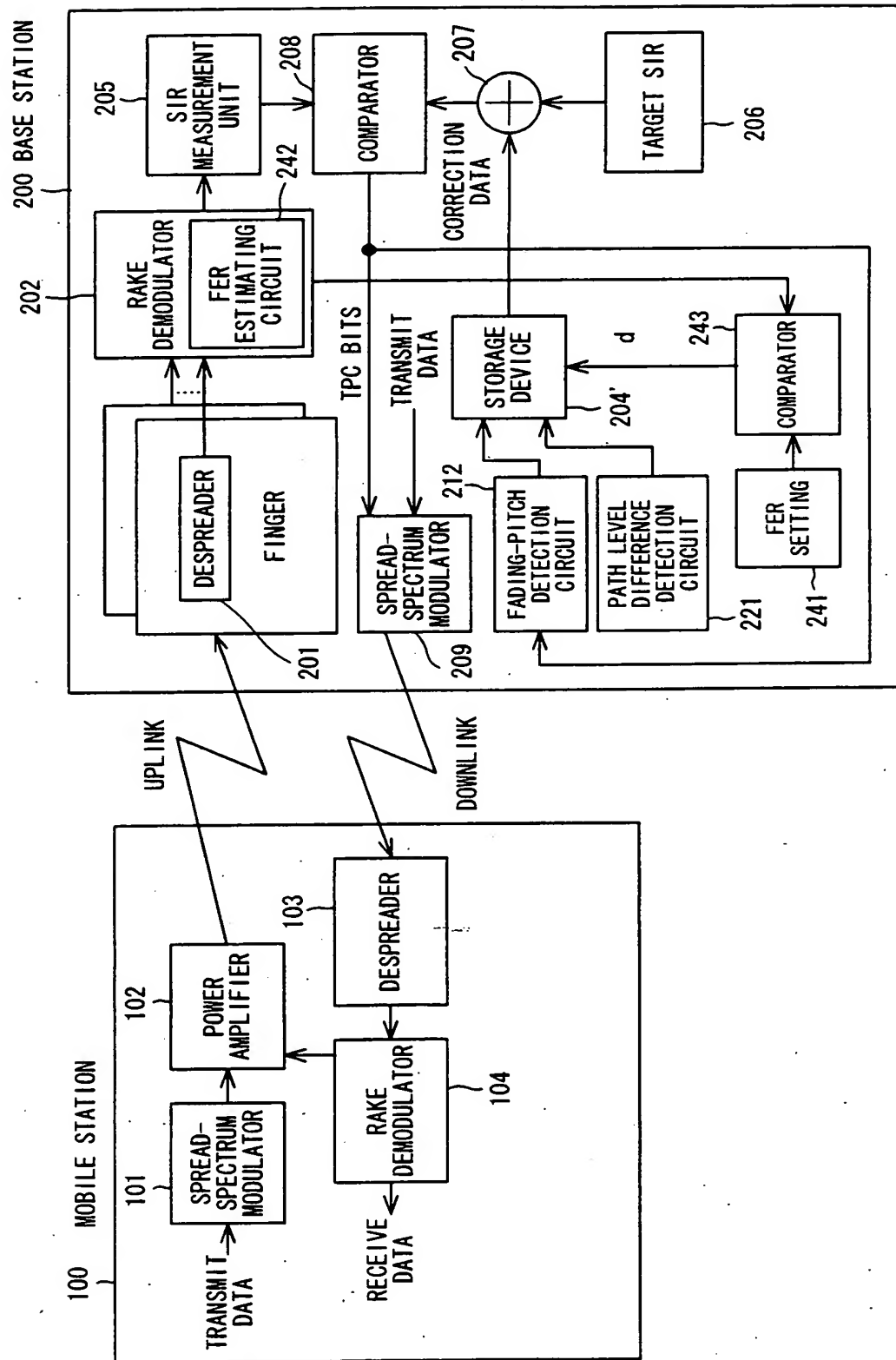
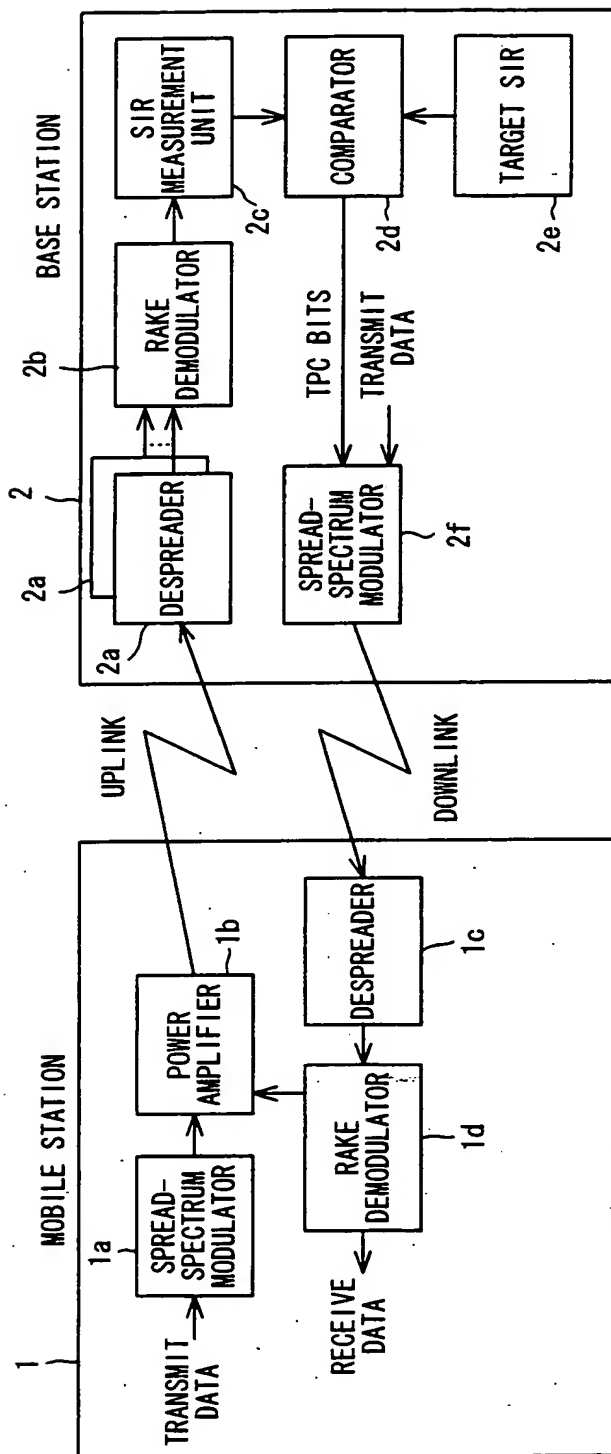


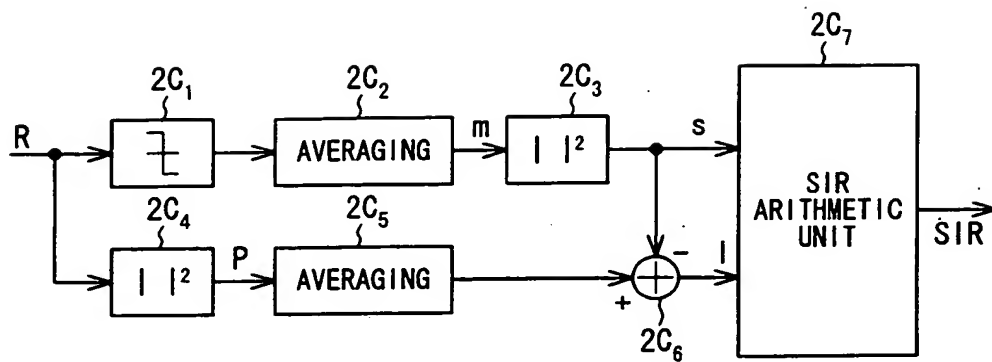
FIG. 25



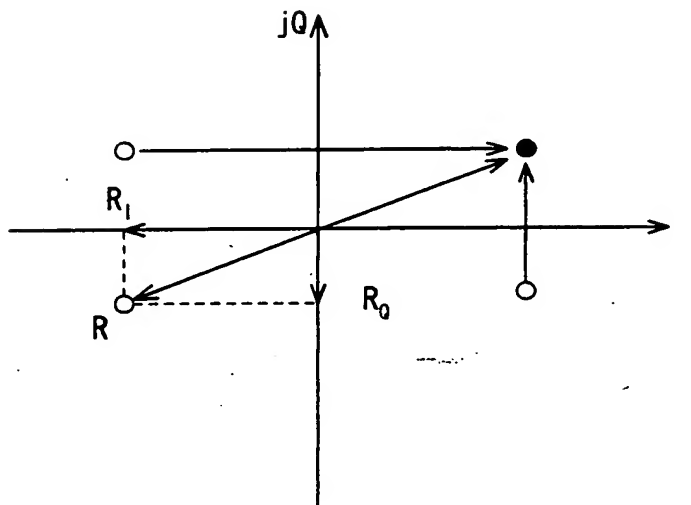
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FIG. 26

(a)

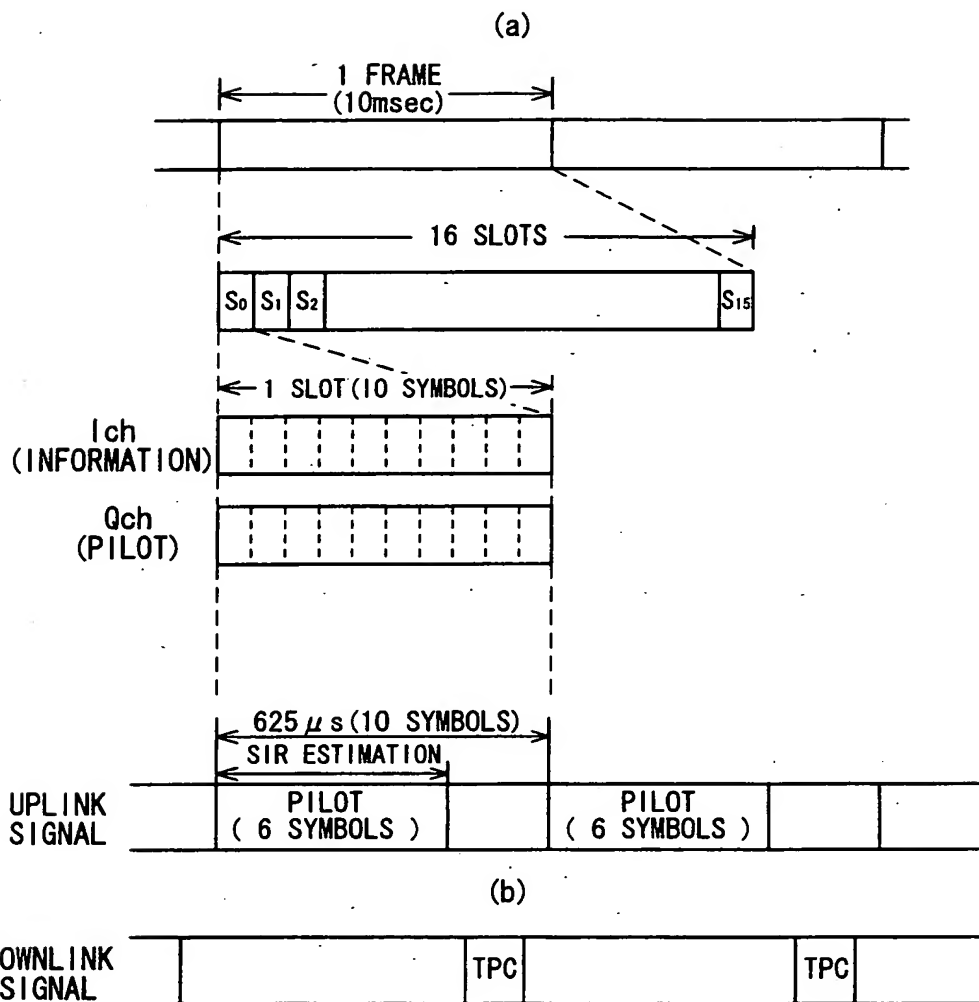


(b)



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FIG. 27



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